

Study on On-Chip Antenna Design Based on Metamaterial-Inspired and Substrate-Integrated Waveguide Properties for Millimetre-Wave and THz Integrated-Circuit Applications

Mohammad Alibakhshikenari¹, Bal S. Virdee², Ayman Abdulhadi Althuwayb³, Sonia Aïssa⁴, Chan H. See⁵, Raed A. Abd-Alhameed⁶, Francisco Falcone^{7,8} and Ernesto Limiti¹

¹Electronic Engineering Department, University of Rome “Tor Vergata”, Via del Politecnico 1, 00133, Rome, Italy

²London Metropolitan University, Center for Communications Technology, London N7 8DB, UK

³Electrical Engineering Department, Jouf University, Sakaka, Aljouf 72388, Kingdom of Saudi Arabia

⁴Institut National de la Recherche Scientifique (INRS), University of Quebec, Montreal, QC, H5A 1K6, Canada

⁵School of Eng. & the Built Environment, Edinburgh Napier University, 10 Colinton Rd., Edinburgh, EH10 5DT, UK

⁶Faculty of Engineering & Informatics, University of Bradford, Bradford, West Yorkshire, BD7 1DP, UK

⁷Electric, Electronic and Communication Engineering Department, Public University of Navarre, 31006 Pamplona, Spain

⁸Institute of Smart Cities, Public University of Navarre, 31006 Pamplona, Spain

Corresponding author: Dr. M. Alibakhshikenari (e-mail: alibakhshikenari@ing.uniroma2.it)

Abstract: This paper presents the results of a study on improving the performance parameters such as the impedance bandwidth, radiation gain and efficiency, as well as suppressing substrate loss of an innovative antenna for on-chip implementation for millimetre-wave and terahertz integrated-circuits. This was achieved by using the metamaterial and the substrate-integrated waveguide (SIW) technologies. The on-chip antenna structure comprises five alternating layers of metallization and silicon. An array of circular radiation patches with metamaterial-inspired crossed-shaped slots are etched on the top metallization layer below which is a silicon layer whose bottom surface is metalized to create a ground-plane. Implemented in the silicon layer below is a cavity above which is no ground-plane. Underneath this silicon layer is where an open-ended microstrip feedline is located which is used to excite the antenna. The feed mechanism is based on the coupling the electromagnetic energy from the bottom silicon layer to the top circular patches through the cavity. To suppress surface-waves and reduce substrate loss SIW concept is applied at the top silicon layer by implementing the metallic via-holes at the periphery of the structure that connect the top layer to the ground-plane. The proposed on-chip antenna has an average measured radiation gain and efficiency of 6.9 dBi and 53%, respectively, over its operational frequency range from 0.285-0.325 THz. The proposed on-chip antenna has dimensions of 1.35×1×0.06 mm³. The antenna is shown to be viable for applications in millimetre-waves and terahertz integrated-circuits.

Keywords: On-chip antenna, terahertz (THz) integrated-circuits, metamaterial (MTM), substrate-integrated waveguide (SIW), silicon process, millimetre-waves (mm-waves), antenna feed mechanism.

I. INTRODUCTION

This is an era of millimeter-wave (mm-wave) and terahertz (THz) wireless communications, which is necessary to deliver multi-Gbps data rates using standard, low-cost integrated circuit technology. THz regime of the electromagnetic spectrum is located between the microwave and optical frequencies and normally defined as the band from 0.1 to 10 THz [1–3]. Currently, industry is commercializing the unlicensed 60 GHz wireless band (e.g. IEEE 802.11ad/WiGig) for indoor short-range communication networks [1-5]. The atmospheric attenuation property of 60 GHz was one of the driving forces for regulatory agencies such as the U.S. FCC to unlicense the multi-GHz of bandwidth at 60 GHz [6]. Beyond 60 GHz more research is needed on how to design and develop THz on-chip antennas [7-12].

Active components functioning at mm-wave and THz circuits are highly integrated except for the antennas [13, 14]. Antenna integration is of great importance [15, 16].

At these frequencies, the antennas need to be assembled using expensive high frequency ground-signal-ground (GSG) probes, bulky waveguides, and horn antennas, which is not conducive for mass production and future industry application. For high-efficiency and gain, the off-chip antenna in the package design is usually fabricated on either the printed circuit board (PCB) [17], low-temperature cofired ceramic (LTCC) [15], or low-loss materials [17]. At mm-wave and THz frequencies the interconnect loss of the packaging is significant (~2 dB at 60 GHz) because of the incompatibility of the antennas and the silicon based active circuits [18-21].

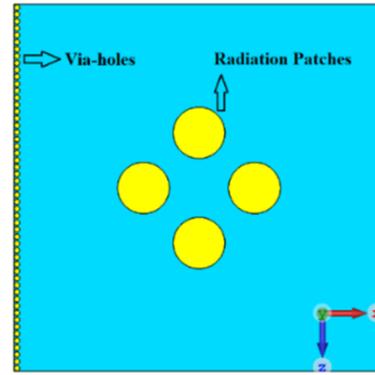
In this paper, an on-chip antenna design is presented for millimetre-wave and THz applications that is constructed from five alternating layers of metallization and silicon. The antenna's performance in terms of impedance bandwidth, radiation gain and efficiency are enhanced by employing the metamaterial (MTM) inspired technology [22-24]. Surface-waves and loss in the silicon substrate are mitigated using substrate integrated

waveguide (SIW) technology [25, 26]. A simple method based on open-ended microstrip-line is employed to excite the antenna. The next section describes the on-chip antenna structure design along with the simulated and measured results, and the paper is finally concluded.

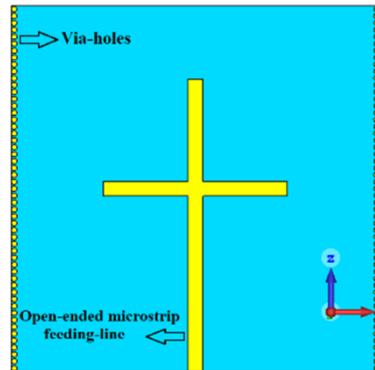
II. HIGH PERFORMANCE ON-CHIP ANTENNA FOR APPLICATIONS IN MM-WAVE AND THZ INTEGRATED-CIRCUITS

Configuration of the reference on-chip antenna in Fig.1 comprises five layers consisting of metallization-silicon-metallization-silicon-metallization. The silicon layers have a dielectric constant of 11.7 and loss-tangent of 0.00025 [27]. Overall fabrication process used here is based on CMOS technology. Fabricated in the top silicon layer are four conventional circular radiation patches. Conductive material used for the radiation patches and the ground-plane is aluminium. A circular cavity is created in the bottom silicon layer under the four circular patches, and the ground-plane over this region is removed. The patches are excited by an open-ended microstrip-line in the form of a cross shaped line that is constructed on the back side of the bottom silicon layer. In this way, the four circular patches on the top layer are aligned with the feedline to maximise coupling. The feeding mechanism is based on coupling the electromagnetic energy from the bottom silicon layer to the top radiation patches through the cavity whose dominant resonance mode is $TE_{11\delta}^z$. The proposed feed mechanism improves the antenna's impedance matching and consequently its impedance bandwidth and radiation characteristics. The periphery of the top silicon layer is punctuated with metallic via-holes to actualize substrate-integrated waveguide (SIW) and thereby suppress surface-waves and minimize substrate loss. Analysis showed that the radius of the metallic via-holes and their spacing from each other are very important to realise low substrates loss and suppress surface-waves. The radius of the via-holes and their separation were $9.0\mu\text{m}$ and $3.5\mu\text{m}$, respectively.

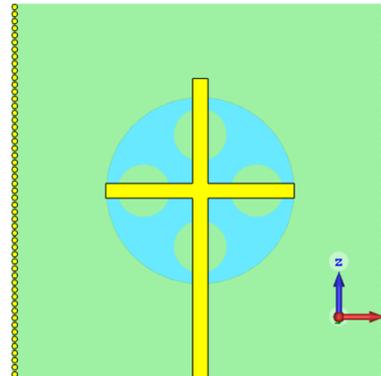
To increase the performance of the antenna its effective aperture area is enlarged without affecting its physical size by applying the metamaterial concept, as illustrated in Fig.2. In this approach, an optimized cross-shaped slot is created inside each circular patch. The periodic array of subwavelength slots act like resonators or scatters that exhibits metamaterial left-handed properties (negative refractive index) when interacting with EM-fields. The resulting structure is referred to as a metasurface, which is a 2D form of a metamaterial [28-30]. The effective permittivity (ϵ) and effective permeability (μ) of the metamaterials when analysed using retrieval extraction algorithm show the structure exhibits negative permittivity over the frequency range of interest, which is a unique characteristic of metamaterials. The physical parameters of the proposed on-chip antenna for optimum performances over 0.285 THz to 0.325 THz are tabulated in Table I.



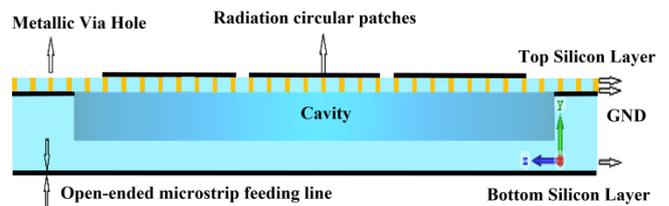
(a) Top-view



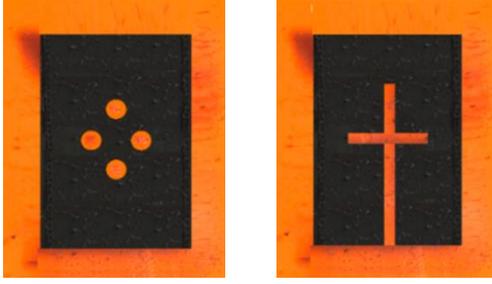
(b) Back-view



(c) View showing relative positions of the feeding line on the bottom layer, the radiation patches on the top layer, and the cavity in the bottom silicon substrate. The cross-shaped feedline is located under the radiation patches to maximise coupling.



(d) Cross-section view showing the various layers of the on-chip antenna structure.

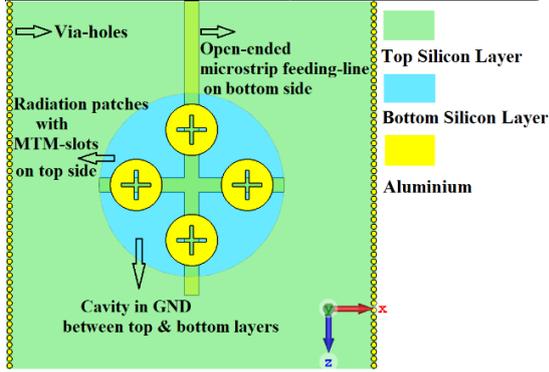


(e) Fabricated prototype, top-view (left-side) and back-view (right-side)

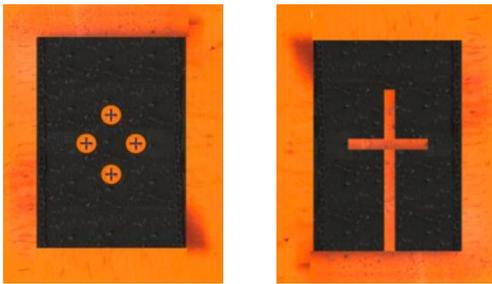
Fig. 1. Configuration of the proposed reference on-chip antenna.

TABLE I. Dimensions of Structural Parameters.

On-chip antenna size	1350×1000×60 μm^3
Thickness of top silicon	5 μm
Thickness of bottom silicon	50 μm
Thickness of GND	5 μm
Radius of cavity	400 μm
Radius of via holes	9 μm
Spacing between via holes	3.5 μm
Radius of circular patches	70 μm
Length of MTM slots	85 μm
Width of MTM slots	10 μm
Length of feeding line	1100 μm
Width of feeding line	100 μm



(a) Simulated layout (top-view)



(b) Fabricated prototype, top-view (left-side) and back-view (right-side)

Fig. 2. Proposed on-chip antenna with metamaterial-inspired crossed-shaped slot implemented on the radiation patches.

The proposed structure was modelled and simulated using CST Microwave Studio, which is a 3-D electromagnetic solver based on finite integration technique. The antenna was then fabricated to validate its performance. The antenna's feedline was excited using WR3 transition using in-line Fin-lines. By using antipodal Fin-lines, shown in Fig.3, a wide range of impedance values can be realized. The impedance match can be

accomplished by tuning the Fin-line dimensions (L and S) and by tapering the two fins to form microstrip signal line and ground-plane, respectively. The tapered fins gradually allow a change from the rectangular waveguide impedance to the microstrip impedance. Hence, the length and shape of the taper determine reflection and operating bandwidth.

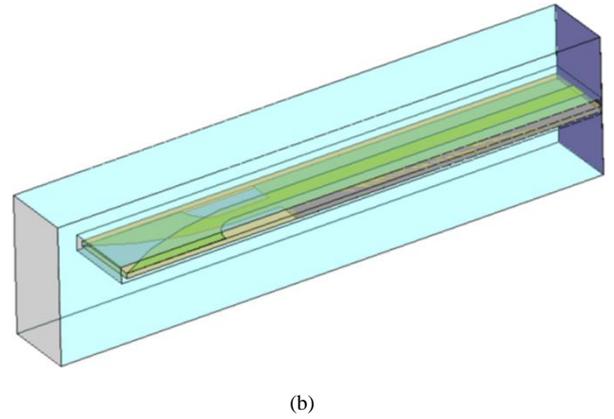
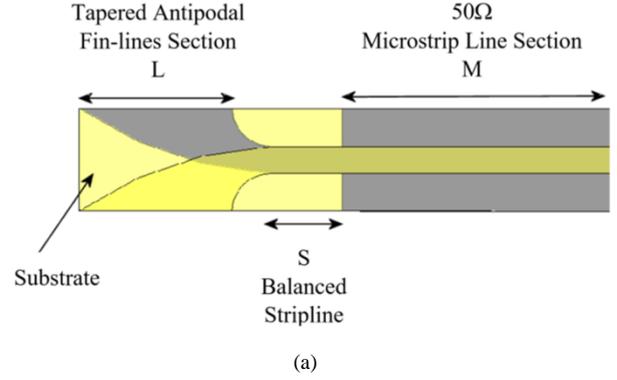


Fig.3 Antipodal Fin-line transition(a) consists of three sections: Fin-line tapers L , balanced microstrip S and microstrip line M . The Antipodal Fin-line transition is located at the centre line of the waveguide broad walls (b).

A 3D plot of the E-field relative to the transition mechanism of antipodal Fin-line at 0.305 THz is shown in Fig.4 highlighting the E-field intensity pattern in the three cascaded sections. The waveguide TE_{10} mode, coupled to the structure as its input, splits at the Fin-line taper point and finally converts into the microstrip line mode.

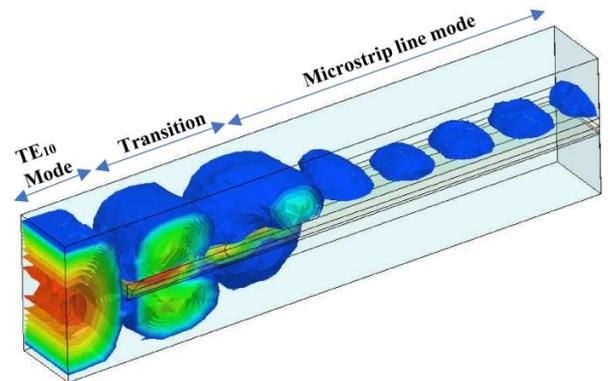


Fig.4 E-field distribution at 0.305 THz. The TE_{10} mode entering the transition from left is split, rotated and finally matched to the microstrip quasi-TEM mode.

The simulated and measured reflection-coefficient response of the reference antenna with no MTM and the proposed antenna with MTM-inspired cross-shaped slots are shown in Fig.5. It is evident that with MTM the impedance match and impedance bandwidth are significantly improved. The proposed structure is shown to effectively operate over the frequency range from 0.285 THz to 0.325 THz for $S_{11} < -15$ dB, which corresponds to a fractional bandwidth of 13.11%.

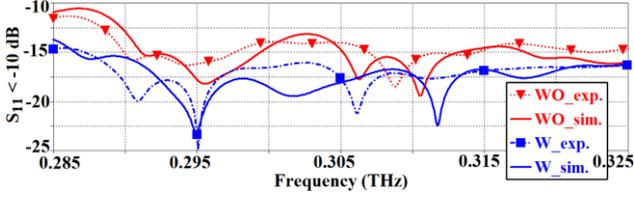
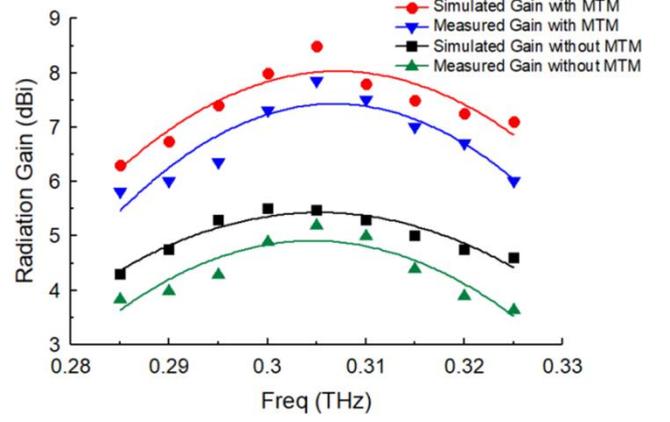


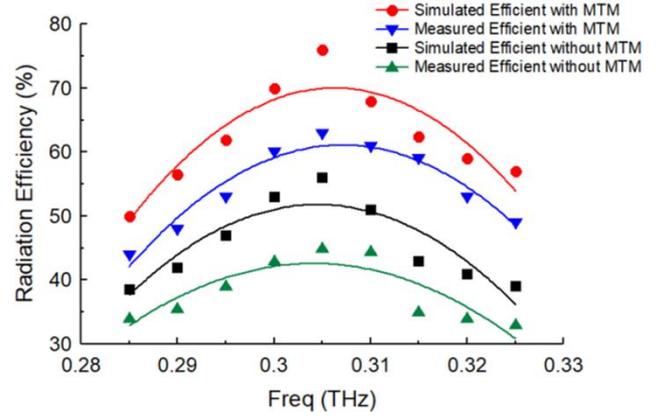
Fig.5. Simulated (sim.) and experimental (exp.) reflection coefficient responses of the reference antenna with no MTM (WO) and proposed on-chip antennas with MTM (W).

The simulated and measured radiation gain and efficiency performances of the reference antenna with no MTM and the proposed antenna with MTM are shown in Fig.6. It is evident that the proposed antenna structure with MTM properties exhibits improvement in the measured gain by 2.4 dBi and radiation efficiency by 14%, which is achieved with no increase in antenna's physical dimensions. The measured average radiation gain and efficiency of the proposed on-chip antenna operating between 0.285 THz to 0.325 THz are 6.9 dBi and 53%, respectively. Performance characteristics of the reference and proposed antenna are summarized in Table II. There is good coherence between the simulation and the measurement in results presented in Figs. 5 & 6, and the discrepancy can be attributed to several factors, namely, imprecise simulation models at terahertz, fabrication tolerances and unwanted signal reflections from surrounding objects during measurements.

The simulated and measured E-plane and H-plane radiation patterns of the proposed metamaterial on-chip antenna at spot frequencies of 0.285, 0.305, and 0.325 THz are shown in Fig.7. This figure shows that in the E-plane the 3-dB beamwidth narrows at the mid-band frequency of 0.305 THz. It also shows the radiation in the E-plane rotates by 90° in the clockwise direction from 0.285 THz to 0.305 THz, and again from 0.305 THz to 0.325 THz. In the H-plane the beamwidth narrows significantly in the mid-band frequency of 0.325 THz.



(a) Radiation gain

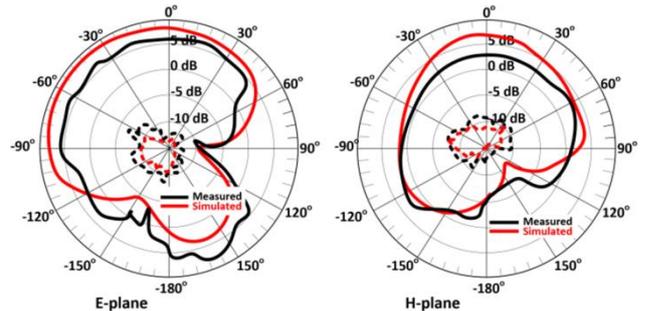


(b) Radiation efficiency

Fig.6. Simulated and measured radiation gain and efficiency over the operating frequency range of the proposed on-chip antenna with and without MTM properties.

TABLE II. Measured Radiation Gain & Efficiency Performance of the On-Chip Antennas With and Without MTM-Inspired Technology

Reference on-chip antenna without MTM properties	
Min. Gain & Efficiency @ 0.325 THz	3.65 dBi & 33.12%
Max. Gain & Efficiency @ 0.305 THz	5.33 dBi & 46.43%
Ave. Gain & Eff.(0.285 THz – 0.325 THz)	4.5 dBi & 39%
Proposed on-chip antenna with MTM properties	
Min. Gain & Efficiency @ 0.285 THz	5.86 dBi & 44.10%
Max. Gain & Efficiency @ 0.305 THz	8.05 dBi & 62.95%
Ave. Gain & Eff. (0.285 THz–0.325 THz)	6.9 dBi & 53%
Improvements after applying MTM properties	
Min. Gain & Efficiency	2.21 dBi & ~11%
Max. Gain & Efficiency	2.72 dBi & 16.52%
Ave. Gain & Efficiency	2.4 dBi & 14%



(a) 0.285 THz

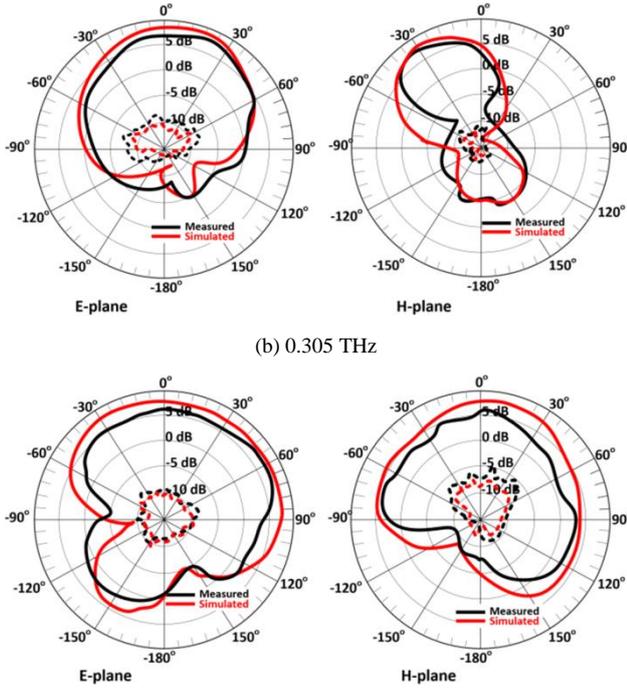


Fig.7. Simulated and measured E-plane and H-plane radiation patterns of the proposed metamaterial on-chip antenna at various spot frequencies in the antenna's operating frequency range. Solid lines represent co-polarization, and dotted lines cross-polarization.

Table III compares the characteristics of the proposed on-chip antenna with other techniques. With the proposed technique a better fractional bandwidth can be achieved. The gain and efficiency of the proposed antenna is comparable to other techniques and in some cases better. In addition, compared to previously reported on-chip antenna designs the proposed design is of a simpler structure and easy to fabricate at low cost, which makes it viable for mass production.

TABLE III. COMPARISON OF THE PROPOSED ON-CHIP ANTENNA WITH THE RECENT PUBLICATIONS

Ref.	Antenna Type	Operation Mode	Freq. / BW (GHz / %)	Gain (dBi)	Eff. (%)	Fab. Process	DR Material	DR Type	Size (mm ²)	Height (mm)
[7]	Patch fed higher order mode DRA	TE ₀₁₇	341 / 7	7.9	74	0.18- μ m SiGe	11.9	Rectangular	0.2	0.5
[8]	On-chip 3D (Yagi like concept)	TE ₁₁₆	340 / 12	10	80	0.13- μ m SiGe	10	Rectangular	0.49	0.43
[10]	Slot loaded magnetic loop on SIW	-	340 / 7	3.3	45	0.13- μ m SMOS	NA	NA	0.49	-
[31]	Patch	-	280 / 2.5	-1.6	21	0.13- μ m CMOS	NA	NA	0.2	-
[32]	Ring antenna	-	296 / -	4.2	-	65-nm CMOS	NA	NA	0.3	-
[33]	Slot ring antenna + superstrate	-	375 / 8	1.6	35	45-nm CMOS SOI	NA	NA	0.05	-
[34]	Ring antenna with silicon lens	-	288 / NA	18.3	65	65-nm CMOS	NA	NA	12.56	2.55
[35] - a	Half-mode cavity fed DRA	TE ₀₁₁	135 / 13	3.7	62	0.18- μ m CMOS	10	Rectangular	0.63	0.25
[35] - b	Half-mode cavity fed higher order mode DRA	TE ₀₁₃ / TE ₀₁₅	135 / 7	6.2 / 7.5	46 / 42	0.18- μ m CMOS	10	Rectangular	0.72	1.3/2.2
[36]	Slot fed stacked DRA	TE ₀₁₁	130 / 11	4.7	43	0.18- μ m CMOS	10	Rectangular	0.72	1.5
[37]	DRA	TE ₀₁₁	135 / 11	2.7	43	0.18- μ m CMOS	10	Rectangular	0.72	0.6
This Work	MTM & SIW	TE ₁₁₆	305 / 13.11	8.05	62.95	0.13- μ m CMOS	NA	NA	2.35	0.06

Note: DR represents Dielectric Resonator, and NR is not applicable.

III. CONCLUSION

The feasibility of the proposed metamaterial-inspired antenna is demonstrated for on-chip applications at the lower end of the THz region. The novelty introduced includes: (i) the feed mechanism for effective coupling of electromagnetic energy from bottom layer to the top radiation patches; (ii) combining metamaterial-inspired and SIW technologies to improve the antenna's performance parameters while preserving its physical dimensions; and (iii) using stacked layers to create a highly compact on-chip antenna structure. The proposed silicon-based antenna structure provides low integration

loss and is relatively simple to design and fabricate and therefore a promising candidate in the millimeter-wave and terahertz integration applications.

ACKNOWLEDGEMENTS

This work is partially supported by RTI2018-095499-B-C31, Funded by Ministerio de Ciencia, Innovación y Universidades, Gobierno de España (MCIU/AEI/FEDER,UE), and innovation programme under grant agreement H2020-MSCA-ITN-2016 SECRET-722424 and the financial support from the UK Engineering and Physical Sciences Research Council (EPSRC) under grant EP/E022936/1.

REFERENCES

- [1] T. S. Rappaport et al., "State of the art in 60-GHz integrated circuits and systems for wireless communications," *Proceedings of the IEEE*, vol. 99, no. 8, Aug. 2011, pp. 1390–1436.
- [2] C. Doan et al., "Millimeter-wave CMOS Design," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, Jan. 2005, pp. 144–155.
- [3] A. Babakhani et al., "A 77-GHz phased-array transceiver with on-chip antennas in silicon: Receiver and antennas," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006, pp. 2795–2806.
- [4] E. Seok et al., "A 410 GHz CMOS push-push oscillator with an on-chip patch antenna," in *2008 IEEE International Solid-State Circuits Conference (ISSCC)*, 3-7 Feb. 2008, pp. 472–629.
- [5] R. Daniels et al., "60 GHz wireless: up close and personal," *IEEE Microwave Magazine*, vol. 11, Dec. 2010, pp. 44–50.
- [6] F. Gutierrez et al., "On-chip integrated antenna structures in CMOS for 60 GHz WPAN systems," *IEEE Journal on Selected Areas in Communications*, vol. 27, Oct. 2009, pp. 1367–1378.
- [7] C.-H. Li and T.-Y. Chiu, "340-GHz low-cost and high-gain on-chip higher order mode dielectric resonator antenna for THz applications," *IEEE Trans. THz Sci. Technol.*, vol. 7, no. 3, May. 2017, pp. 284–294.
- [8] X.-D. Deng, Y. Li, C. Liu, W. Wu and Y. -Z. Xiong, "340 GHz on-chip 3-D antenna with 10 dBi gain and 80% radiation efficiency," *IEEE Trans. THz Sci. Technol.*, vol. 5, no. 4, July. 2015, pp. 619–627
- [9] X.-D. Deng, Y. Li, H. Tang, W. Wu and Y. -Z. Xiong, "Dielectric loaded endfire antennas using standard silicon technology," *IEEE Trans. Ant. Propag.*, vol. 65, no. 6, Jun. 2017, pp. 2797-2807
- [10] X.-D. Deng, Y. Li, W. Wu and Y. -Z. Xiong, "340-GHz SIW cavity-backed magnetic rectangular slot loop antennas and arrays in silicon technology," *IEEE Trans. Ant. Propag.*, vol. 63, no. 12, Dec. 2015, pp. 5272-5279.
- [11] Z. Hou, Y. Yang, X. Zhu, S. Liao, M. Shum and Q. Xue, "A 320 GHz On-Chip Slot Antenna Array Using CBCPW Feeding Network in 0.13- μm SiGe Technology," *IEEE MTT-S Int. Microwave Symposium, Honolulu, Hawaii, Jun. 2017.*
- [12] S. Hu, Y.-Z. Xiong, B. Zhang, L. Wang, T.-G. Lim, M. Je and M. Madhian, "A SiGe BiCMOS transmitter/receiver chipset with on-chip SIW antennas for terahertz applications," *IEEE Jour. Solid-State Cir.*, vol. 47, no. 11, Nov. 2012, pp. 2654-2664.
- [13] A. Tomkins, R. A. Aroca, T. Yamamoto, S. T. Nicolson, Y. Doi, and S. P. Voinigescu, "A zero-IF 60 GHz 65 nm CMOS transceiver with direct BPSK modulation demonstrating up to 6 Gb/s data rates over a 2 m wireless link," *IEEE J. Solid-State Circuits*, vol. 44, Aug. 2009, pp. 2085-99.
- [14] S. T. Nicolson, P. Chevalier, B. Sautreuil, and S. P. Voinigescu, "Single-chip W-band SiGe HBT transceivers and receivers for Doppler radar and millimeter-wave imaging," *IEEE J. Solid-State Circuits*, vol. 43, Oct. 2008, pp. 2206-2217.
- [15] Y. P. Zhang, M. Sun, K. M. Chua, L. L. Wai, and L. Duixian, "Antenna-in-package design for wire bond interconnection to highly integrated 60-GHz radios," *IEEE Trans. Antennas and Propag.*, vol.57, Oct. 2009, pp. 2842-2852.
- [16] S. Hu, Y. Z. Xiong, L. Wang, D. Hou, and T. G. Lim, "A low-cost high-gain antenna array and its integration with active circuits," *IEEE Electrical Design of Advanced Packag. Systems Symp.*, Dec. 2010.
- [17] U. R. Pfeiffer, J. Grzyb, L. Duixian, B. Gaucher, T. Beukema, B. A. Floyd, and S. K. Reynolds, "A chip-scale packaging technology for 60-GHz wireless chipsets," *IEEE Trans. Microw. Theory Tech.*, vol.54, Aug. 2006, pp. 3387-3397.
- [18] J. Li, Y. Z. Xiong, S. Hu, W. L. Goh, D. Hou, and W. Wu, "Performance analyse on millimetre-wave bonding-wire interconnection," *IEEE Electrical Design of Advanced Package. Systems Symp.*, Dec. 2010.
- [19] B. Y. Y. Liu, Y. Ye, J. Ren, X. Liu, and Q. J. Gu, "High efficiency micromachined sub-THz channels for low cost interconnect for planar integrated circuits," *IEEE Trans. on Microwave Theory and Techniques*, vol.64, no.1, Jan. 2016, pp.96-105.
- [20] B. Y. Y. Liu, Y. Ye, X. Liu, and Q. J. Gu, "Low-loss and broadband G-band dielectric interconnect for chip-to-chip communication," *IEEE Microwave & Wireless Components*, vol.26, no.7, July 2016, pp.478-480.
- [21] U. Dey and J. Hesselbarth, "Millimeter-wave multicast chip-to-chip interconnect network using dielectric slab waveguide," *IEEE/MTT-S Int. Microwave Symp.*, 10-15 June 2018, Philadelphia, PA, USA.
- [22] Yuandan Dong, and Tatsuo Itoh, "Metamaterial-Based Antennas", *Proceedings of the IEEE*, Vol. 100, No. 7, July 2012, pp. 2271-2285.
- [23] M. Mohammadi, F. H. Kashani, J. Ghalibafan, A partially ferrite-filled rectangular waveguide with CRLH response and its application to a magnetically scannable antenna, *J. Magn. Magn. Mater.* 491 (2019) 165551.
- [24] Morteza Mohammadi, F. H. Kashani, J. Ghalibafan, Backfire-to-endfire scanning capability of a balanced metamaterial structure based on slotted ferrite-filled waveguide, *Waves Random Complex Media.* (2019) 1-15.
- [25] M. Mohammadi Shirkolaei, J. Ghalibafan, "Unbalanced CRLH behavior of ferrite-loaded waveguide operated below cutoff frequency," *Waves in Random and Complex Media*, 2020.
- [26] K. Wu, Y. J. Cheng, T. Djerafi, and W. Hong, "Substrate-Integrated Millimeter-Wave and Terahertz Antenna Technology", *Proceedings of the IEEE*, vol. 100, no. 7, July 2012, pp. 2219-2232.
- [27] B. Benakaprasad, A. Eblabla, X. Li, D.J. Wallis, I. Guiney, and K. Elgaid, "Design and Performance Comparison of Various Terahertz Microstrip Antennas on GaN-on-Low Resistivity Silicon Substrates for TMIC," *Asia-Pacific Microwave Conference 2016*, pp.1-4.
- [28] C. Caloz and T. Itoh, "Electromagnetic Metamaterials: Transmission Line Theory and Microwave Applications", New York: Wiley-IEEE Press, 2005.
- [29] Y. Dong, and T. Itoh, "Metamaterial-Based Antennas," *Proceedings of the IEEE*, vol. 100, no. 7, pp. 2271-2285, July 2012.
- [30] W. Yang, S. Chen, W. Che, Q. Xue, and Q. Meng, "Compact high-gain metasurface antenna arrays based on higher-mode SIW cavities," *IEEE Transactions on Antennas and Propagation*, vol. 66, no. 9, September 2018, pp. 4918-4923.
- [31] R. Han et al., "A 280-GHz Schottky diode detector in 130-nm digital CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 564–580, Nov. 2011.
- [32] S. Jameson, E. Halpern, and E. Socher, "A 300 GHz wirelessly locked 2x3 array radiating 5.4 dBm with 5.1% DC-to-RF efficiency in 65 nm CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2016, pp. 348–349.
- [33] F. Golcuk, O. D. Gurbuz, and G. M. Rebeiz, "A 0.39-0.44 THz 2x4 amplifier-quadrupler array with peak EIRP of 3-4 dBm," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 12, Dec. 2013, pp. 4483–4491.
- [34] J. Grzyb, Y. Zhao, and U. R. Pfeiffer, "A 288-GHz lens-integrated balanced triple-push source in a 65-nm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 48, no. 7, Jul. 2013, pp. 1751–1761.
- [35] D. Hou et al., "D-band on-chip higher-order-mode dielectric-resonator antennas fed by half-mode cavity in CMOS technology," *IEEE Antennas Propag. Mag.*, vol. 56, no. 3, Jun. 2014, pp. 80–89.
- [36] D. Hou, Y.-Z. Xiong, W.-L. Goh, S. Hu, W. Hong, and M. Madhian, "130-GHz on-chip meander slot antennas with stacked dielectric resonators in standard CMOS technology," *IEEE Trans. Antennas Propag.*, vol. 60, no. 9, Sep. 2012, pp. 4102–4109.
- [37] D. Hou, Y.-Z. Xiong, W. Hong, W.-L. Goh, and J. Chen, "Silicon based on-chip antenna design for millimeter-wave/THz applications," in *Elect. Design of Adv. Pkg. and Syst. Symp. (EDAPS)*, 2011, pp. 1–4.



Mohammad Alibakhshikenari (Member, IEEE) was born in Iran, in 1988. He received the Ph.D. degree (Hons.) in Electronic Engineering from the University of Rome "Tor Vergata", Italy, in February 2020. Dr. Alibakhshikenari was recipient of two years postdoctoral research grant awarded by the Electronic Engineering Department of the University of Rome

"Tor Vergata" in 2019. As well as, he was recipient of International Postgraduate Research (Ph.D.) Scholarship (IPRS) by Italian Government started in 2016 for three years.

In 2018 for eight months, he was working with the Antenna System Division, Department of Electrical Engineering, Chalmers University

of Technology, Gothenburg, Sweden, as a Ph.D. Visiting Researcher. As well as, his training during the Ph.D. included a research stage in the Swedish company Gap Waves AB that is developing components in a technology. He is currently working as a postdoctoral grant holder researcher with the University of Rome "Tor Vergata", Italy. During his Ph.D. research period, he has participated in 14 international IEEE conferences over the world, where he has presented 20 articles mostly in oral presentations. During his Ph.D. degree, he was winner of 13 grants for participating in the European Doctoral Schools on Antennas and Metamaterials organized by several European Universities and European School of Antennas (ESoA). He acts as a referee in several high reputed journals and IEEE international conferences. His research interests include antennas and wave-propagations, phased antenna arrays, metamaterials and metasurfaces, synthetic aperture radars (SAR), multiple-input multiple-output (MIMO) systems, waveguide slotted antenna arrays, substrate integrated waveguides (SIWs), impedance matching networks, on-chip antennas, microwave components, millimeter-waves and terahertz integrated circuits, and electromagnetic systems. The above research lines have produced more than 90 publications on refereed-international journals, presentations within international-conferences, and book chapters with a total number of the citations more than 1100, H-index of 23, and I10-index of 40 reported by the Google Scholar Citation. He was winner of an annual research grant started on November 2019, and to be finalized in November 2020, which has been funded by the Department of Electronic Engineering, University of Rome "Tor Vergata". Dr. Alibakhshikenari was two recipients of the 47th and 48th European Microwave Conference (EuMC) Young Engineer Prize, in 2017, Nuremberg, Germany, and in 2018, Madrid, Spain, where he has presented his articles. He gave an Invited Lecture entitled "Metamaterial Applications to Antenna Systems" at the Department of Information and Telecommunication Engineering, Incheon National University, Incheon, South Korea, which was in conjunction with the 8th Asia-Pacific Conference on Antennas and Propagation (APCAP 2019), where he was the Chair of the Metamaterial session as well. He is serving as a Editorial Board Members for "International Journal of Electrical and Computer Engineering (IJECE)", and Guest Editor for a special issue entitled "Millimeter-wave and Terahertz Applications of Metamaterials" in "Applied Sciences". In April 2020, his article entitled "High-Gain Metasurface in Polyimide On-Chip Antenna Based on CRLH-TL for Sub Terahertz Integrated Circuits" published in "Scientific Reports" was awarded as best month paper at the University of Bradford, U.K.



Bal S. Virdee (SM'08) received the B.Sc. and MPhil degrees in Communications-Engineering from the University of Leeds-UK and his Ph.D. in Electronic-Engineering from the University of London-UK. He has worked in industry for various companies including Philips (UK) as an R&D-engineer and Filtronic-Components Ltd. as a future products developer in the area of RF/microwave communications. He has taught at several academic institutions before joining London Metropolitan University where he is a Professor of Microwave-Communications in the Faculty of Life Sciences&Computing where he Heads the Center for Communications-Technology and is the Director of London Metropolitan-Microwaves. His research, in collaboration with industry and academia, is in the area of microwave wireless communications encompassing mobile-phones to satellite-technology. Prof. Virdee has chaired technical sessions at IEEE international conferences and published numerous research-papers. He is Executive-Member of IET's Technical and Professional Network Committee on RF/Microwave-Technology. He is a Fellow of IET and a Senior-Member of IEEE.



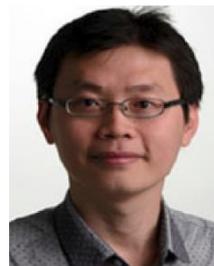
Ayman Abdulhadi Althwayb received the B.Sc. degree (Hons.) in electrical engineering (electronics and communications) from Jouf University, Saudi Arabia, in 2011, the M.Sc. degree in electrical engineering from California State University, Fullerton, CA, USA, in

2015, and the Ph.D. degree in electrical engineering from Southern Methodist University, Dallas, TX, USA, in 2018. He is currently an Assistant Professor with the department of electrical engineering at Jouf University, Kingdom of Saudi Arabia. His current research interests include antenna design and propagation, microwaves and millimeter-waves, wireless power transfer, ultrawideband and multiband antennas, filters and other.



Sonia Aïssa (S'93-M'00-SM'03-F'19) received her Ph.D. degree in Electrical and Computer Engineering from McGill University, Montreal, QC, Canada, in 1998. Since then, she has been with the Institut National de la Recherche Scientifique-Energy, Materials and Telecommunications Center (INRS-EMT), University of Quebec, Montreal, QC, Canada, where she is a Full Professor. From 1996 to 1997, she was a Researcher with the Department of Electronics and

Communications of Kyoto University, and with the Wireless Systems Laboratories of NTT, Japan. From 1998 to 2000, she was a Research Associate at INRS-EMT. In 2000-2002, while she was an Assistant Professor, she was a Principal Investigator in the major program of personal and mobile communications of the Canadian Institute for Telecommunications Research, leading research in radio resource management for wireless networks. From 2004 to 2007, she was an Adjunct Professor with Concordia University, Canada. She was Visiting Invited Professor at Kyoto University, Japan, in 2006, and at Universiti Sains Malaysia, in 2015. Her research interests include the modeling, design and performance analysis of wireless communication systems and networks. Dr. Aïssa is the Founding Chair of the IEEE Women in Engineering Affinity Group in Montreal, 2004-2007; acted as TPC Symposium Chair or Cochair at IEEE ICC '06 '09 '11 '12; Program Cochair at IEEE WCNC 2007; TPC Cochair of IEEE VTC-spring 2013; TPC Symposia Chair of IEEE Globecom 2014; TPC Vice-Chair of IEEE Globecom 2018; and serves as the TPC Chair of IEEE ICC 2021. Her main editorial activities include: Editor, IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS, 2004-2012; Associate Editor and Technical Editor, IEEE COMMUNICATIONS MAGAZINE, 2004-2015; Technical Editor, IEEE WIRELESS COMMUNICATIONS MAGAZINE, 2006-2010; and Associate Editor, Wiley Security and Communication Networks Journal, 2007-2012. She currently serves as Area Editor for the IEEE TRANSACTIONS ON WIRELESS COMMUNICATIONS. Awards to her credit include the NSERC University Faculty Award in 1999; the Quebec Government FRQNT Strategic Faculty Fellowship in 2001-2006; the INRS-EMT Performance Award multiple times since 2004, for outstanding achievements in research, teaching and service; and the Technical Community Service Award from the FRQNT Centre for Advanced Systems and Technologies in Communications, 2007. She is co-recipient of five IEEE Best Paper Awards and of the 2012 IEICE Best Paper Award; and recipient of NSERC Discovery Accelerator Supplement Award. She served as Distinguished Lecturer of the IEEE Communications Society and Member of its Board of Governors in 2013-2016 and 2014-2016, respectively. Professor Aïssa is a Fellow of the Canadian Academy of Engineering.



Chan Hwang See (M'14, SM'15) received a first class B.Eng. Honours degree in Electronic, Telecommunication and Computer Engineering and a Ph.D. degree from the University of Bradford, UK in 2002 and 2007, respectively. He is an associate Professor and Head of Electrical Engineering and Mathematics in School of Engineering and the Built Environment, Edinburgh Napier University, UK. Previously, he was a Senior Lecturer (Programme Leader) in Electrical &

Electronic Engineering, School of Engineering, University of Bolton, UK. He also is a Visiting Research Fellow in School of Engineering and Informatics, University of Bradford, UK. Prior to this, he was a Senior

Research Fellow in the Antennas and Applied Electromagnetics Research Group within the University of Bradford. His research interests cover wireless sensor network system design, computational electromagnetism, antennas and acoustic sensor design. He has published over 200 peer-reviewed journal articles and conference papers in the areas of antennas, computational electromagnetics, microwave circuits, acoustic sensors and wireless sensor system designs. He is a co-author for one book and three book chapters. He was a recipient of two Young Scientist Awards from the International Union of Radio Science (URSI) and Asia-Pacific Radio Science Conference (AP-RASC) in 2008 and 2010, respectively. He was awarded a certificate of excellence for his successful Knowledge Transfer Partnership (KTP) with Yorkshire Water on the design and implementation of a wireless sensor system for sewerage infrastructure monitoring in 2009. Dr. See is a Chartered Engineer, Fellow of the Institution of Engineering and Technology. He is also a Fellow of the Higher Education Academy and Associate Editor for IEEE Access.



Raed A. Abd-Alhameed (M'02–SM'13) received the B.Sc. and M.Sc. degrees from Basrah University, Basrah, Iraq, in 1982 and 1985, respectively, and the Ph.D. degree from the University of Bradford, Bradford, U.K., in 1997, all in electrical engineering. He is a Professor of electromagnetic and radio frequency engineering at the University of Bradford. He has long years' research experience in the areas of radio frequency, signal processing,

propagations, antennas, and electromagnetic computational techniques, and has published more than 500 academic journal and conference papers; in addition, he is a coauthor of three books and several book chapters. He is currently the Leader of Radio Frequency, Propagation, Sensor Design, and Signal Processing; in addition to leading the Communications research group for years within the School of Engineering and Informatics, Bradford University. He is a Principal Investigator for several funded applications to EPSRCs and leader of several successful Knowledge Transfer Programmes (KTPs) such as with Arris (previously known as Pace plc), Yorkshire Water plc, Harvard Engineering plc, IETG Ltd., Seven Technologies Group, Emkay Ltd., and Two World Ltd. He has also been a Co-Investigator in several funded research projects including: H2020 MARIE Skłodowska-CURIE ACTIONS: Innovative Training Networks “Secure Network Coding for Next Generation Mobile Small Cells 5G-US,” nonlinear and demodulation mechanisms in biological tissue (Department of Health, Mobile Telecommunications & Health Research Programme, and Assessment of the Potential Direct Effects of Cellular Phones on the Nervous System (EU: collaboration with six other major research organizations across Europe). He received the Business Innovation Award for his successful KTP with Pace and Datong companies on the design and implementation of MIMO sensor systems and antenna array design for service localizations. He is the Chair of several successful workshops on Energy Efficient and Reconfigurable Transceivers: Approach Towards Energy Conservation and CO₂ Reduction that addresses the biggest challenges for future wireless systems. He was also appointed as a Guest Editor for IET Science, Measurements and Technology in 2009 and 2012. He has also been a Research Visitor at Glyndwr University, Wrexham, U.K., since September 2009, covering the wireless and communications research areas. His research interests include computational methods and optimizations, wireless and mobile communications, sensor design, EMC, beam steering antennas, energy-efficient PAs, and RF predistorter design applications. Dr. Abd-Alhameed is the Fellow of the Institution of Engineering and Technology, U.K., a Fellow of the Higher Education Academy, and a Chartered Engineer in the U.K.



Francisco Falcone (M'05, SM'09) received the degree in telecommunication engineering and the Ph.D. degree in communication engineering from the Universidad Pública de Navarra (UPNA), Spain, in 1999 and 2005, respectively. From February 1999 to April 2000, he was the Microwave Commissioning Engineer at Siemens-Italtel, deploying microwave access systems. From May 2000 to

December 2008, he was a Radio Access Engineer at Telefónica Móviles, performing radio network planning and optimization tasks in mobile network deployment. In January 2009, as a co-founding member, he has been the Director of Tafco Metawireless, a spin-off company from UPNA, until May 2009. In parallel, he is an Assistant Lecturer with the Electrical and Electronic Engineering Department, UPNA, from February 2003 to May 2009. In June 2009, he becomes an Associate Professor with the EE Department, being the Department Head, from January 2012 to July 2018. From January 2018 to May 2018, he was a Visiting Professor with the Kuwait College of Science and Technology, Kuwait. He is also affiliated with the Institute for Smart Cities (ISC), UPNA, which hosts around 140 researchers. He is currently acting as the Head of the ICT Section. His research interests are related to computational electromagnetics applied to the analysis of complex electromagnetic scenarios, with a focus on the analysis, design, and implementation of heterogeneous wireless networks to enable context-aware environments. He has over 500 contributions in indexed international journals, book chapters, and conference contributions. He has been awarded the CST 2003 and CST 2005 Best Paper Award, the Ph.D. Award from the Colegio Oficial de Ingenieros de Telecomunicación (COIT), in 2006, the Doctoral Award UPNA, 2010, 1st Juan Gomez Peñalver Research Award from the Royal Academy of Engineering of Spain, in 2010, the XII Talgo Innovation Award 2012, the IEEE 2014 Best Paper Award, 2014, the ECSA-3 Best Paper Award, 2016, and the ECSA-4 Best Paper Award, 2017.



Ernesto Limiti (S'87–M'92–SM'17) is a full professor of Electronics in the Engineering Faculty of the University of Roma Tor Vergata since 2002, after being research and teaching assistant (since 1991) and associate professor (since 1998) in the same University. Ernesto Limiti represents University of Roma Tor Vergata in the governing body of the MECSA (Microwave Engineering Center for Space Applications), an inter-university center

among several Italian Universities. He has been elected to represent the Industrial Engineering sector in the Academic Senate of the University for the period 2007–2010 and 2010–2013. Ernesto Limiti is actually the president of the Consortium “Advanced research and Engineering for Space”, ARES, formed between the University and two companies. Further, he is actually the president of the Laurea and Laurea Magistrale degrees in Electronic Engineering of the University of Roma Tor Vergata. The research activity of Ernesto Limiti is focused on three main lines, all of them belonging to the microwave and millimetre-wave electronics research area. The first one is related to characterisation and modelling for active and passive microwave and millimetre-wave devices. Regarding active devices, the research line is oriented to the small-signal, noise and large signal modelling. Regarding passive devices, equivalent-circuit models have been developed for interacting discontinuities in microstrip, for typical MMIC passive components (MIM capacitors) and to waveguide/coplanar waveguide transitions analysis and design. For active devices, new methodologies have been developed for the noise characterisation and the subsequent modelling, and equivalent-circuit modelling strategies have been implemented both for small and large-signal operating regimes for GaAs, GaN, SiC, Si, InP MESFET/HEMT devices. The second line is related to design methodologies and characterisation methods for low noise circuits. The main focus is on cryogenic amplifiers and devices. Collaborations are currently ongoing with the major radioastronomy institutes all around Europe within the frame of FP6 and FP7 programmes (RadioNet). Finally, the third line is in the analysis methods for nonlinear microwave circuits. In this line, novel analysis methods (Spectral Balance) are developed, together with the stability analysis of the solutions making use of traditional (harmonic balance) approaches. The above research lines have produced more than 250 publications on refereed international journals and presentations within international conferences. Ernesto Limiti acts as a referee of international journals of the microwave and millimetre wave electronics sector and is in the steering committee of international conferences and workshops. He is actively involved in research activities with many research groups, both European and Italian, and he is in tight collaborations with high-tech Italian (Selex - SI, Thales Alenia Space, Rheinmetall, Elettronica S.p.A., Space Engineering ...) and foreign (OMMIC, Siemens, UMS, ...) companies. He contributed, as a researcher and/or as unit responsible, to several National (PRIN MIUR, Madess CNR, Agenzia Spaziale Italiana)

and international (ESPRIT COSMIC, Manpower, Edge, Special Action MEPI, ESA, EUROPA, Korrigan, RadioNet FP6 and FP7 ...) projects. Regarding teaching activities, Ernesto Limiti teaches, over his institutional duties in the frame of the Corso di Laurea Magistrale in Ingegneria Elettronica, "Elettronica per lo Spazio" within the Master Course in Sistemi Avanzati di Comunicazione e Navigazione Satellitare. He is a member of the committee of the PhD program in Telecommunications and Microelectronics at the University of Roma Tor Vergata, tutoring an average of four PhD candidates per year.