A Hybrid Inverter System for Medium Voltage Applications using a Low Voltage Auxiliary CSI

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Abstract—**Hybrid converters consist of a main inverter processing the bulk of the power with poor waveform performance and a fast and versatile auxiliary inverter to correct the distortion. In this paper, the main converter is a medium voltage NPC inverter and the auxiliary inverter is a low-voltage and low-current rated current source inverter (CSI), with series capacitor being used to minimize the CSI voltage stress. The result is a high output current quality which is obtained with a very low switching stress in the main converter and a very small added installed power (<4%) in the CSI. This paper expands this concept by investigating the hybridization of a medium voltage inverter with an existing LCL filter and investigates the additional challenges related to resonances and proposes a solution for stabile operation.**

I. INTRODUCTION

Conversion of DC into AC at medium and high voltage levels has become a very important research topic now when the need to transfer very large amounts of power (GW) over long distances favor HVDC transmission systems. In the medium term it is predicted that the distribution system will remain AC which will require the use of high voltage DC/AC inverters to interface the transmission and distribution systems. Standard two-level inverters built using series connected devices were initially used in the first generation of forced commutated HVDC systems for their simplicity and the easiness to embed redundancy by adding additional devices in series; however, difficulties in achieving static and more importantly dynamic voltage sharing during switching meant that the harmonic performance of such inverters was poor due to reduced voltage levels and further limited by the low switching frequency. In the last 5 years, forced commutated IGBTs with ratings of 6.5kV became commercially available which would reduce the number of series connected devices needed in a two-level inverter and therefore lower complexity and cost. However, the poorer switching performance of a medium voltage (voltage rating >2kV) forced commutated device which for same kVA switched, results in higher switching loss, is also a limiting factor that will limit the switching frequency to approximately 1 kHz, which means power quality will remain a problem for a two-level medium/high voltage inverter implementation.

Multilevel voltage inverter topologies [1] such as the cascaded H-bridge, the flying capacitor and the diode clamped inverters proposed more than 15 years ago, promised to solve the limitations of the inverters using series connected switches but their application was limited in practice to a low number of levels (three as is the case of the NPC inverter). The most important drawbacks were that the modulation and control became very complex and also that building of an inverter leg with high number of levels requiring different connection paths for the clamping diodes or capacitors that resulted in large and uneven stray inductances made the implementation of building blocks quite difficult. The Modular Multilevel Converter (MMC) proposed few years ago [2] has gained increased popularity in a short period of time due to its reliance on a large number of identical building blocks that would enable cost effective mass production and allow flexibility in implementing any custom design system solutions. Hybrid converter implementations have been proposed in the past to enhance the behavior of passive filters [3] or to improve the waveform quality of slow converters by adding low current rated auxiliary converters [4]-[7].

In [7] the authors of this paper have proposed a hybrid solution aimed at improving the harmonic performance of a slow switching medium/high voltage inverter by means of employing an auxiliary current source inverter with very low installed power to cancel the switching harmonics caused by the main converter. The CSI is used because it is very good at synthesizing an AC current reference, in this case the switching current ripple which is in the hundreds Hz range of the main MV inverter, with the lowest switching frequency. A series capacitor to block most of the fundamental (50Hz) voltage is connected in series with the CSI to minimize its voltage ratings so standard/fast switches (ratings up to 1.2kV) could be used.
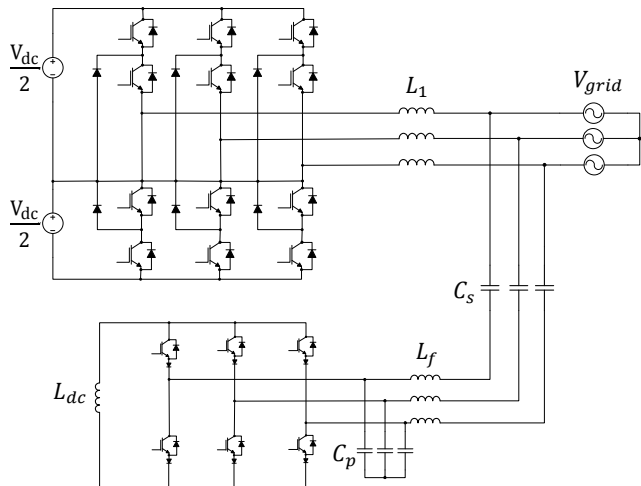
Figure 1: Hybrid converter topology connected to a stiff grid

Figure 2: Hybrid converter topology with LCL filter interconnection

The proposed hybrid concept shown in Fig. 1 is similar to [4] where the auxiliary inverter cancels the main current switching ripple which is a fraction of the main inverter current. With respect to the hybrid filter idea, most papers are using a Voltage Source Inverter as the auxiliary bridge which if used to synthesize currents would require a fast current controller and for that reason very fast switching.

[5] has demonstrated the idea of implementing a medium voltage active filter by using a low voltage 3-phase voltage source active power filter (APF) in series with a capacitor to minimize/block the 50Hz fundamental component voltage stress across the converter whilst also minimizing the cost. The use of a series capacitor with a CSI has been investigated in [6] but for low voltage APF applications. The novelty in relation to [4] is that it addresses medium/high voltage applications and that the installed power of the auxiliary inverter is further reduced by using a series connected capacitor to cancel most of the fundamental (50Hz) AC voltage, similar to [5]. By using a current source inverter (CSI) as in [6] the circuit does not need the current controllers that a VSI would need in an active filter application, since the AC reference currents are synthetized directly, therefore, being able to switch slower for a similar current tracking performance.

The second section of this paper briefly outlines the design procedure followed in [7] for the Hybrid converter in a medium voltage stiff grid application, revealing the key results and system scaling considered necessary for the reader to familiarize with the context and operation of the Hybrid concept. The third section outlines the procedure followed into designing the LCL filter and CSI along with the design considerations taken and alterations compared to the previous design. The forth section outlines the options for damping resonant frequencies and proposes an active damping compensator before showing the simulation results that validate the expected operation of the hybrid system.
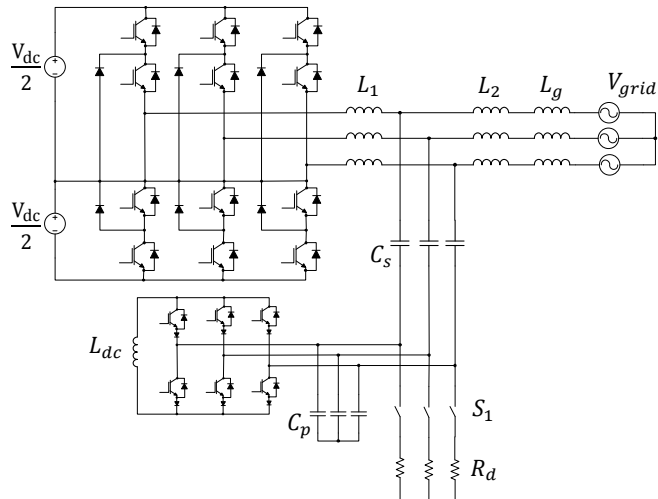
II. LCL CONNECTED HYBRID TOPOLOGY

This paper expands on previous work relating to the Hybrid concept in [7] by investigating the challenges of applying the same technique to connect the auxiliary CSI via series capacitors to the MV grid/main inverter via their split inductance that typically will form an LCL filter and lead to the known associated stability problems reported already in literature [8]. The resulting topology is shown in Fig. 2. It contains also a set of damping resistors and a contactor that can be used to switch the main VSI operation mode from passive LCL filtering of the switching current ripple to active/hybrid operation.

The evolution from the Hybrid topology shown in Fig. 1, which assumes an ideal stiff grid, to the LCL connected Hybrid topology in Fig. 2 comes as a logical progression when taking into account the supply line inductance. This could be considered a more realistic implementation for medium voltage (and perhaps weaker) grids, as the grid line inductance will naturally form an output LCL filter when combined with the series capacitance and VSI side inductance. The other advantage is that the inductor L_f present in the CSI filter shown in Fig. 1 is no longer necessary.

LCL filters are known to achieve better attenuation compared to a 1st order (L) filter with smaller component size however their design is more challenging due to the need to carefully consider the resonant frequency placement and the potential damping of resonances. LCL filter design for medium voltage applications is even more restricted by the low converter switching (around 1kHz) frequency [9]-[10] therefore requiring the filter resonant frequency to be placed close to the typical low order harmonics(5th, 7th etc) present in distribution grids. The problem is outlined in [9] where the concept of virtual harmonic content is introduced in order to design the LCL filter to comply with grid code requirements with the lowest possible filter size whilst [10]

proposed the additional use of the computationally demanding selective harmonic elimination PWM (SHE-PWM) to eliminate harmonics up to the 29th order to allow for higher resonant frequency placement and therefore achieve smaller filter size. Although in this paper, a more simplistic approach was taken towards the LCL filter design, the considerations are in line with existing literature [8]-[10].

The connection of the CSI operating as an Active Power Filter (APF) on an existing LCL filter can achieve further harmonic current improvement with very low added installed power with the highlighted possibility of adding only the CSI and its AC side filter capacitor C_p with no other additional components or modifications needed. The resulting topology shown in Fig. 2 allows for two modes of operation via switch S1. When the switch is closed and the CSI disabled, the VSI operates using passive LCL filtering with the resistors R_d providing damping. When the switch is opened and the CSI is enabled, the circuit operates as a Hybrid active filter with the damping resistor R_d and its associated losses removed. As a result the overall topology can be considered hybrid in two ways, due to the combination of a main VSI and auxiliary CSI as well as the option of choosing between passive and active filtering.

Switch S1 in this simulation study is used to compare the harmonic performance between passive and active filtering. Realistically it could be implemented as a mechanical or electronic (triac) switch depending on the functionality needed: redundancy or safe startup/shut-down.

The addition of the CSI to the LCL has two main topological implications. During active filtering, the damping resistor R_d of the LCL filter is no longer needed therefore a source of resistive losses is removed. Compared to the stiff grid design, the AC side filter inductor of the CSI (L_f) are no longer necessary as sufficient attenuation is achieved by the combination of capacitor C_p and grid side inductance. The unexpected benefit of this is that, when using a stiff grid connection this filter favored high CSI switching frequencies to maintain small component size. However, as the large enough grid side inductance is present in an LCL filter, a lower switching frequency of the CSI can give the same performance.

III. DESIGN OF THE HYBRID SYSTEM CONNECTED TO A STIFF/IDEAL GRID

The circuit topology, shown in Fig. 1, consists of a slow switching medium voltage three level Neutral Point Clamped (NPC) VSI as the main bridge that interconnects with the MV grid via a line side inductance L_1 that is designed to limit the switching current ripple while the Series Capacitor Active Power Filter APF auxiliary bridge is a three phase two level CSI connected in series with a capacitor (C_s) that is designed to block most of the 50Hz voltage. Capacitor C_p along with L_f and R_f (not shown) is the CSI second order low-pass AC side filter necessary to smooth the PWM output

current of the APF. The control of the main VSI is independent to the CSI and can remain largely unchanged compared to a standalone VSI installation. The CSI primary role is to act as an active filter to the switching current ripple produced by the VSI. By also injecting a calculated fundamental current in the series capacitor it is possible to control the fundamental voltage drop on the capacitor and therefore ensure minimal voltage stress on the CSI. The reference waveform to the CSI is therefore the switching current ripple of the main bridge which can be sensed and the calculated reactive fundamental current component to achieve the desired voltage drop. The detailed hybrid converter model including the phasorial diagrams used to derive the control and the design equations are detailed in [7]. In Table I, the specifications for the hybrid converter used in this simulation study are summarised.

TABLE I: SPECIFICATIONS FOR MEDIUM VOLTAGE HYBRID SYSTEM DESIGN

$V_{g\,L-L}$	I_g	$V_{g\,ph}$	Vdc	S	ΔI_{mc}	f_{sw}^{VSI}	f_{sw}^{CSI}
3.3 kVrms	330 Arms	2.7 kVpk	2x3 kV	1.89 MVA	94 A	1 kHz	30 kHz

A. Design Procedure Outline

The converter side inductance L_1 has been designed by limiting the maximum current ripple in the inverter side inductance L_1 to 20% of the peak to peak maximum current. This maximum current ripple is calculated based on the VSI DC link voltage level and the modulating strategy chosen for a given topology.
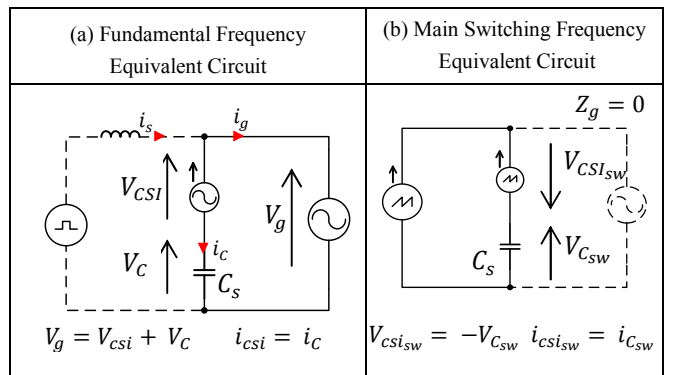

Fig. 3. Simplified phase equivalent circuit at
a) the fundamental grid frequency and b) VSI switching frequency

Fig. 3 reveals the simplified phase equivalent circuit at the fundamental and VSI switching frequency. The series capacitor C_s design is designed based on various requirements. A smaller series capacitance results in lower reactive current requirement to achieve a given fundamental voltage drop however this is counteracted by the larger switching voltage drop (2) across the series capacitor which is mirrored equally at the AC side of the CSI as shown in Fig. 3b. To ensure that the series capacitance meets the design requirements, the minimum value is calculated based on (3) for a maximum switching voltage stress while the maximum value is based on limiting the maximum reactive

power requirement on the VSI (4) to minimise the effect on the output power factor.

$$V_{csi}{}_{sw}^{ln} = |i_{sw}|X_c = \frac{|i_{sw}|}{\omega_{sw}C_s} = -V_{c}{}_{sw}^{ln} \quad (2)$$

$$C_{s_{min}} = \frac{|i_{sw}|}{\omega_{sw}|V_{csw}|} \quad (3)$$

$$C_{s_{max}} = \left(\frac{Q}{S}\right)\frac{\sqrt{3}i_s^{RMS}}{V_g^{RMS}\omega} \quad (4)$$

The parallel capacitance C_p is chosen to be large enough to smooth the CSI PWM current however must be kept as small as possible to reduce the amount of circulating current which is based on the ratio of series and parallel capacitances (5). The switching current reference to the CSI must be multiplied by a gain (5) to compensate for that bleeding current. The inductance L_f and resistance R_f are subsequently chosen to form a second order low pass filter with cut off frequency at half the CSI switching frequency or less in order to achieve sufficient attenuation. In this case the filter has been designed for a cut-off frequency of 10 kHz.

$$G = 1 + \frac{C_p}{C_s} \quad (5)$$

The maximum voltage stress on the CSI has been chosen as 20% of the peak grid voltage (940$V_{\text{L-L-pk}}$), with half being caused by the fundamental voltage (V_g-V_{Cs}) and the other half (10%) caused by the switching current ripple across C_s which is mirrored also across the CSI AC input. This design scenario results in the minimum value for C_s. Limiting the reactive power as percentage (20%) of the apparent power defines the other limit for the series capacitor range, which in this case is 55-110μF. In Table II shows all the parameters for the design procedure with stiff grid.

TABLE II: DESIGN PARAMETERS FOR HYBRID CONVERTER WITH STIFF/IDEAL GRID

C_s min	C_s max	L_f	R_f	L_{dc}
55μF	110μF	23μH	10Ω	20mH
C_p	L_1	V_{sw} max @55 μF	V_{csi} max	I_{dc} @ C_s @55/110 μF
11μF	3.6mH	470V	940Vpk	140/184

B. Control Scheme of the Hybrid Converter

The control of the CSI is implemented according to the diagram shown in Fig 4. The switching current ripple is extracted from VSI inductor L_1 current per phase, removing any low order harmonics or DC components and multiplied by (5) to compensate for the fraction of the CSI current that is trapped by the CSI filter capacitors C_p. The fundamental current component is calculated in the *dq* rotating frame with the active component contributing towards maintaining the DC-link current above the peak of the AC current reference and the reactive component to achieve the desired capacitor voltage drop and synchronised with the grid voltage. Finally a DC voltage compensator is added to protect the CSI and series capacitor voltages from the possibility of DC drifting.
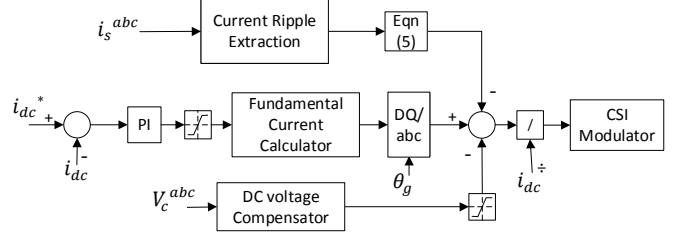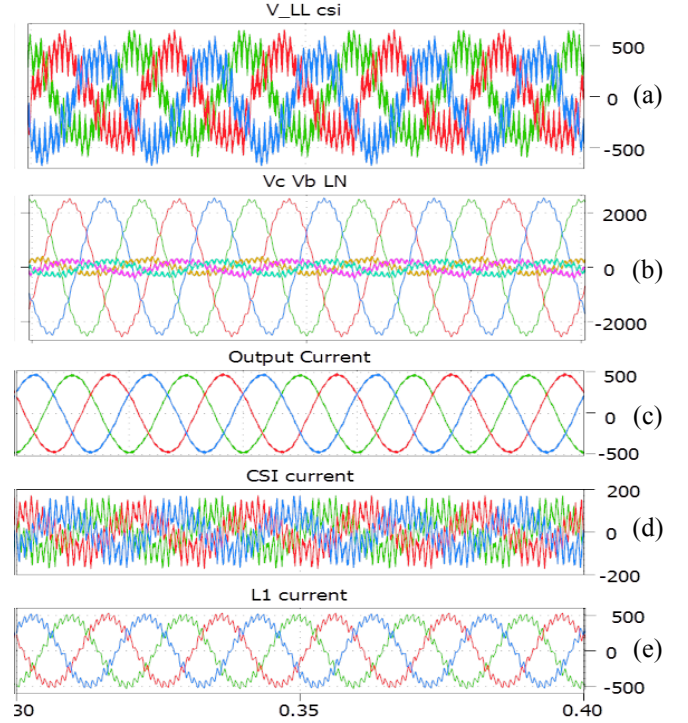

Fig. 4. Control scheme overview

Fig. 5. Hybrid converter connected to a stiff grid: a) AC L-L voltages of the CSI; b) Series capacitor (large) and CSI phase voltages; c) resulting grid currents; d) injected currents by the CSI; e) main VSI currents.

C. Simulation results of Hybrid Converter with stiff grid

The simulation results of the hybrid converter operating with stiff grid are presented in Fig 5 for a series capacitance of 110μF. The CSI maximum voltage stress is below 20% of the line to line grid voltage with the Capacitor and CSI phase voltages shown together in Fig. 5b, for comparison. The grid current THD has been calculated at 2% compared to 11% THD of the VSI side current, achieving a 96% reduction in the main switching frequency harmonic and all current harmonics being kept below 1% of the fundamental current. The installed power in the CSI is maintained below 4%.

IV. HYBRID SYSTEM CONNECTED VIA LCL FILTER

The following section outlines the additional design considerations along with the procedure required to obtain a stable performance when the hybrid converter is connected to the grid via an LCL filter under the same requirements for the maximum CSI voltage stress and grid specifications.

Since the system in Fig 2 can operate as two different circuits, they will be treated as such in the design procedure and referred to as Passive mode, when the switch S1 is closed and CSI is disabled and Active mode when S1 is open and CSI is enabled. The procedure starts by designing the LCL circuit, ensuring proper Passive mode operation. The focus of the paper is afterwards centred on the design of the CSI and the choices made in order to meet the aforementioned design requirements.

The single phase equivalent circuits for each mode are shown in Fig. 6 where the inductances of the LCL output and grid side (L_2 and L_g) are grouped as a single inductance L_o to reflect the frequency response of the system.

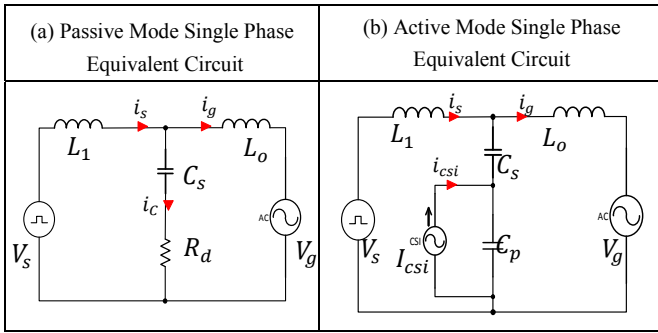| (a) Passive Mode Single Phase Equivalent Circuit	(b) Active Mode Single Phase Equivalent Circuit

Fig. 6. Single Phase equivalent circuits for a) Passive; b) Active Filtering

A. LCL Filter Design Procedure

The VSI inductance L_1 is chosen to limit maximum switching current ripple at 20% giving the same value as in the stiff grid situation of 3.6mH. The Grid side impedance is then calculated based on [11] for a *SCR*= 10 and *X/R* = 5 resulting in L_g=1.8mH and R_g=0.113Ω. This values have been chosen to be representative of a near weak grid situation, usually identified as having a SCR lower than 10, to reflect the possibility of the system operating in non-ideal grid situations. The inductance L_2 is chosen at 1.8mH so that L_g+L_2 matches the converter side inductance therefore avoiding extra resonances in the system.

The LCL/series capacitor C_s must then be chosen to place the resonant frequency (6) at approximately half of the switching frequency or below. The maximum capacitance value is usually restricted based on the allowed reactive power generated therefore a similar range of capacitances for C_s can be considered as the previous design i.e. 55-110µF with respective resonant frequencies between 500-360Hz

$$\omega_{res1} = \frac{1}{\sqrt{L_t C_s}} \quad \text{where } L_t = \frac{L_1 L_o}{L_1 + L_o} \quad (6)$$

For the following design, a value of 100µF has been chosen to place the resonant frequency at 375Hz. A damping resistor R_d=50mΩ to give sufficient damping and very good attenuation of the 1 kHz switching frequency ripple.

B. CSI Active filter design

The connection of the CSI and its filter capacitor C_p in neutral point of the LCL filter presents a convenient place from the point of view of maintaining low voltage insulation and voltage CSI ratings, as the neutral potential is closest to ground but leads to an intriguing design problem to provide stable operation. In addition to the CSI design restrictions existent for the stiff grid connection, the placement of the new resonant frequency needs careful consideration as it may be significantly higher, influenced by a smaller capacitance (C_p). For a 10:1 C_s/C_p ratio, the new resonant frequency may three times higher than for the passive LCL.

The problem can be explained by considering the harmonic current spectrum produced by the VSI that needs to be removed. The triangular shape of the current ripple means that the first harmonic will cause the largest sidebands around the switching frequency and the remaining harmonic clusters situated around multiples of the switching frequency with negligible amplitudes above 5kHz.
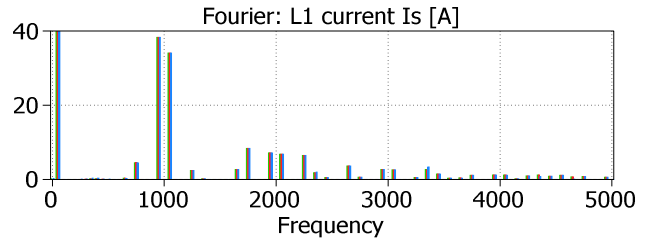

Fig. 7. VSI (L1) inductor current harmonics

In a stiff grid situation, the CSI design is implemented by matching the parallel capacitance Cp as a fraction of Cs to limit the circulating current and then choosing an appropriate filter inductance to place the cut-off frequency at less than half of the CSI switching frequency (typically 10-15 kHz for 30kHz CSI switching frequency). This means that the CSI filter produces no/constant attenuation for the VSI current ripple (f<5kHz) to be cancelled (Fig.7).

In the LCL scenario, the connection of capacitance C_p to C_s will mitigate the resonant frequency of the LCL filter. Fig. 8 illustrates the resonant frequency mitigation by showing the Bode plot of converter voltage V_s to current I_s with the corresponding resonances for active and passive mode.

$$\omega_{r1} = \frac{1}{\sqrt{L_t C_s}} \quad \omega_{r2} = \frac{1}{\sqrt{L_1 C_s}}$$

$$\omega_{r3} = \frac{1}{\sqrt{L_t C_t}} \quad \omega_{r4} = \frac{1}{\sqrt{L_1 C_t}}$$
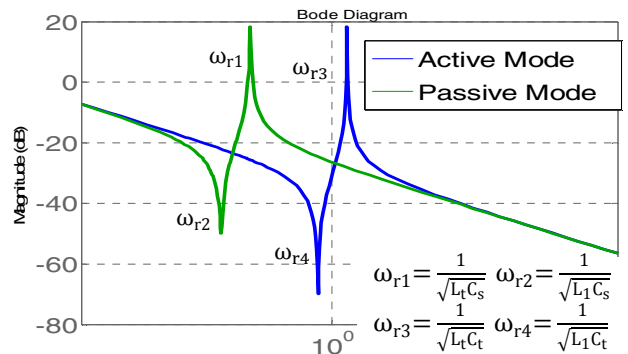
Fig. 8. Converter Voltage to Converter Current Bode plot for active and passive filtering mode. (the frequency scale is logarithmic in [kHz])

Considering that the resonant frequency of a medium voltage LCL filter is typically situated around half of the most significant lowest switching frequency harmonic, it makes it impossible to place the new resonant frequency ω_{r3} outside of the current harmonic range to be cancelled shown in Fig. 7. Placing the resonance below the switching frequency sidebands is impossible as it would require a much larger capacitance ratio compared to C_s and placing the resonance above 5 kHz is also not feasible as the capacitance would be too small causing large switching harmonic voltage across it.

The capacitance value must therefore be selected to avoid placing the resonant frequency where a switching current harmonic is situated as this could excite resonance and would create instability. In this case the suggested value would be near 1.5 kHz, equally spaced between the harmonic clusters of the switching frequency and twice switching frequency. For the following design however C_p has been chosen at 10µF placing the resonant frequency at 1190Hz, close to the 1250Hz sideband in order to demonstrate that stable circuit operation is possible under certain damping options which means the component design is not so strict.

C. Passive damping

One option of dealing with resonance is via the use of passive damping. Fig. 9 reveals three possible damping options and Fig. 10 shows the corresponding frequency response on the input voltage to input current for the values listed below.
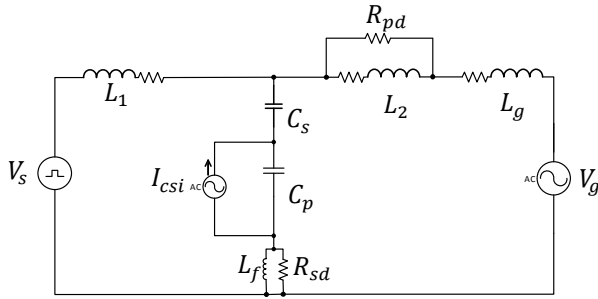

Fig. 9. Single Phase Equivalent circuit showing passive damping options
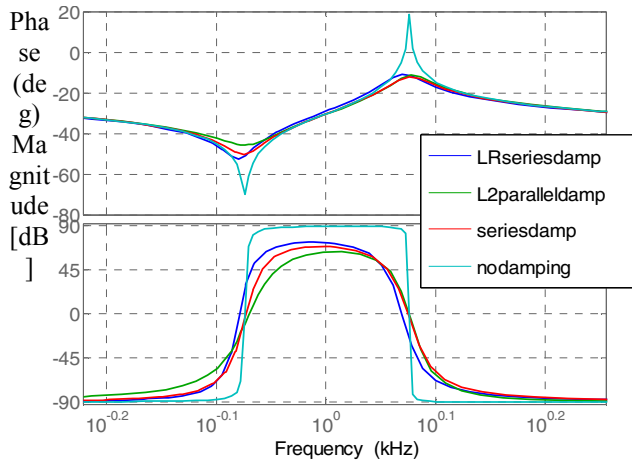

Fig. 10. Frequency response under different passive damping scenarios

- L_2 parallel damping resistor $R_{pd} =50\Omega$
- Series capacitor damping resistor $R_{sd} =1\Omega$
- Series capacitor LR damping $R_{sd} =1\Omega$, $L_f =0.3$mH

The option of adding a parallel resistance to L_2 is effective, but as the parallel resistor cannot be removed during passive mode the losses are increased. Thus one of the other two methods could be pursued with the advantage that if critical damping can be achieved, the CSI control circuit remains the same as in the stiff grid situation. Realistically, some damping is achieved by the internal AC resistance of the components, which for high current rating inductors (L_1, L_2, L_g) may have significant skin effect around 1kHz. But the addition of extra damping resistance would lead to additional cost and losses, making passive damping undesired.

D. Active damping

The high switching frequency and application of the CSI in this hybrid topology to cancel the switching disturbance means that any resonance which is situated within the bandwidth of the controller should theoretically be contained by default. The placement of the resonant frequency within the current spectrum of harmonics to be eliminated means that using only the gain stated in (5) is no longer sufficient and that the frequency characteristic of the CSI to grid current needs to be considered in order to achieve stability.

This task however is not straightforward due to the associated phase characteristic at around the resonant frequency. Unlike active damping requirements in other applications which are focused mainly on the reduction of the gain characteristic at the resonant frequency, this application requires that the phase characteristic of the converter side current must be maintained and reproduced accurately in order for the ripple cancellation to take place. As a result a closed loop control system approach must be put in place to achieve unity gain and zero phase characteristic throughout the frequency range of interest.

Fig. 11 shows the proposed active damping control system while Fig 12 shows separately, the corresponding Bode plots of the Plant (I_c/I_{csi}), of the resonance compensator and of the overall closed loop response. The switching current ripple extracted from the main converter (L_1) current i_s is the reference signal for the series capacitor current i_c. The resonance compensator acts as a notch filter at the resonant frequency as shown in Fig 12. The controller is designed so that the closed loop response behaves like a low pass filter with cut-off frequency around 15kHz and zero or negligible phase shift up to 5kHz. The actual implementation means that the "Eq (5)" block in Fig. 4 is replaced with the resonance compensator.
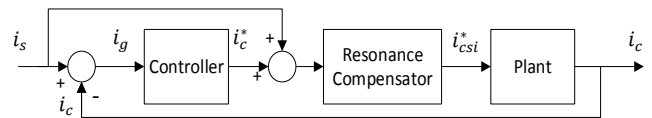

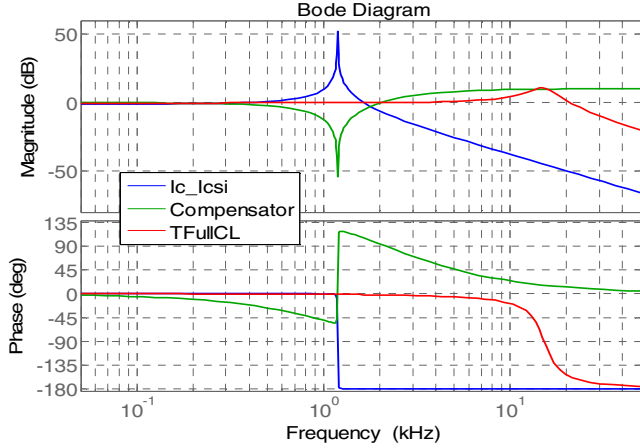Fig. 11. Active damping implementation for Ripple Cancellation

Fig. 12. Bode plots of the following transfer functions: Icsi to Ic, the resonance compensator and the overall closed loop active damped system

V. SIMULATION RESULTS

The performance evaluation of the proposed hybrid system shown in Fig. 2 is carried out by implementing its simulation model and the control in Plecs. One aspect has been simplified, by placing an ideal current source instead of an inductance in the DC-link of the CSI. But the d-component of the reference CSI current is forced to zero to make sure that the auxiliary CSI does not contribute with active power.

Steady state and transient operation are tested and the simulated results are shown and discussed in this section. Fig. 13 shows the currents injected in the grid and the VSI output current when the converter operates in LCL passive damping mode. Even though the most switching ripple is removed, slight disturbance of the grid currents is visible. Fig. 14 shows that the voltages seen on the AC side of the CSI when the hybrid converter operates in active filtering mode, are below 1kV, in line with the design.
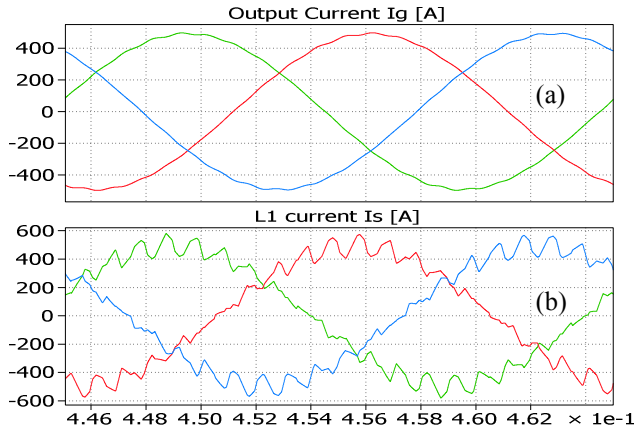

Fig. 13. LCL passive mode: a) Grid currents and b) VSI output currents

Fig. 15 reveals the transient performance of the system when operation is changed from passive LCL filtering mode ($t<0.28s$) to activation of the CSI ($t_1=0.28s$) followed by a rapid build-up of resonance of the LC circuit that include the small CSI filter capacitor C_f and result in a resonant frequency in the proximity of the upper switching sideband

which makes things worse but was deliberately chosen to demonstrate the effectiveness of the active damping compensator which is activated at $t_2=0.36$ and facilitates full damping of the resonance ($t>0.7s$) without involving any dissipative element (damping resistance).

In order to assess accurately the performance, the grid currents were sampled at key moments during this transient and the resulting grid current FFTs are shown in Fig. 13b-d. It can be observed that passive LCL filtering mode offers a good power quality with the highest switching harmonic being reduced from $38A_{pk}$ (Fig. 7) to 3.2Apk which means by almost 12 times (-21.5dB). A residual current harmonic is present at approx. 750Hz that corresponds to the resonance frequency of the LC circuit formed by the grid/main inverter inductance and the series capacitor C_s. The X/R ratio considered however, provides sufficient damping to this circuit and the resonant harmonic stays reasonably low.

When active filtering is enabled and after the resonance damped, it can be noticed that same switching harmonic considered before (950Hz) is reduced to $1.1A_{pk}$ which by a factor of 34.5 (-30.8dB). However, the most important harmonic is the upper sideband which peaks at 1.8A which corresponds to a smaller attenuation compared to Fig. 7 and the cause is that the active damping compensator of the LC filter having a resonance at 1.25kHz, very close to the upper side that needs to be attenuated, is altering the active filter behaviour of the circuit. This can be improved by increasing the CSI filter capacitor so that the resultant resonant frequency is moved at 1.5 kHz, equally spaced between upper switching frequency sideband and lower twice the switching frequency sideband. This would minimise the interaction between the resonant compensator and the active filter at the relevant switching harmonics. It should be noted that the CSI voltages reveal that during steady state operation the voltages remain below 20% of the grid voltage, within the design requirements.
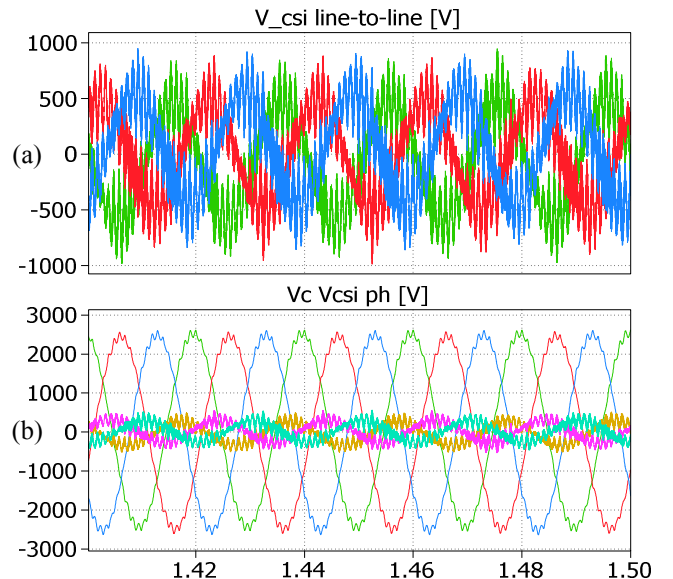

Fig. 14. a) CSI line-to-line voltages and b) series capacitor voltages and phase-neutral CSI voltages
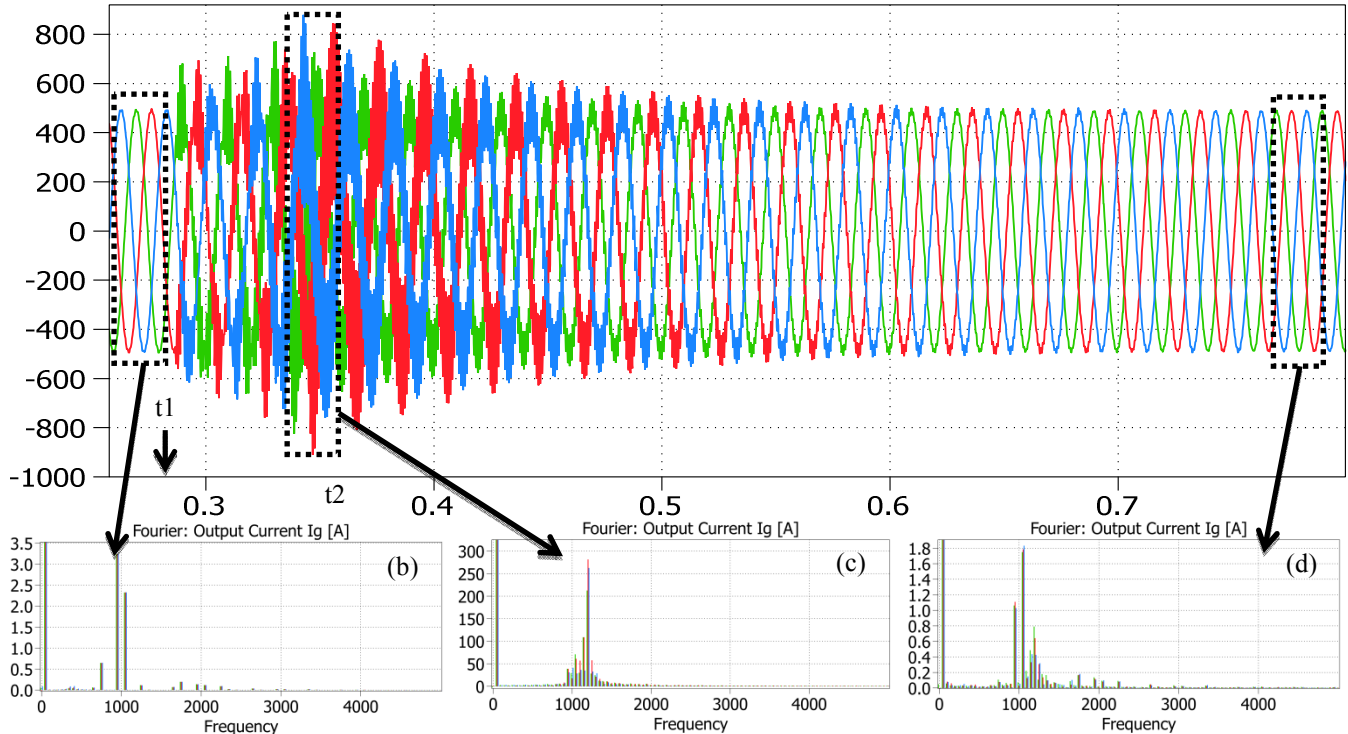
Fig. 15. Transient operation showing activation of CSI at t1=0.28s followed by LC circuit resonance build-up and activation of the resonance compensator at t2=0.36s followed by resonance being actively damped (t>0.7s). b)-c)-d) FFT of the MV grid currents when b) CSI was off and switching ripple is passively damped by the LCL filter; c) just before active damping activation (t=0.34-0.36); d) at end of simulation when resonance levels are not visible.

V. CONCLUSIONS

This paper validates the feasibility of the hybrid concept resulting by adding a CSI to a medium voltage LCL filter to enhance the switching ripple cancellation while maintaining low installed power on the CSI. The design criteria to achieve low installed power in the CSI that are defining the design of the hybrid system with a stiff grid have been introduced and validated by simulations.

The LCL-CSI connection scenario which is relevant for upgrading existing MV inverter installations introduces some new design challenges related to LC resonance, which have been outlined in this paper. To address this challenge, a resonance compensator that behaves similar to a notch filter on the resonance but guarantees zero phase-shift in the frequency range of interest for the switching ripple has been added to the control diagram.

To validate the effectiveness of the proposed resonance compensator, the resonant frequency of the hybrid system has been intentionally placed near the biggest VSI current harmonics in order to demonstrate that the design requirements are not strict as long as the compensator is properly designed but the attenuation performance of the switching ripple nearest to the resonant frequency is affected. This is proven via a set of transient simulation tests by enabling the resonance compensator after the CSI was enabled and a resonance has build-up, followed by an effective removal of the resonance after the compensator was activated.

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